Laboratory #10
Output Stages

I. Objectives

1. Master the fundamentals of the output stages
2. Understand the definition of the conversion efficiency

II. Components and Instruments

1. Components
   (1) Signal NPN transistor: 2N2222 ×2
   (2) Signal PNP transistor: 2N3906 ×1
   (3) Resistor: 10Ω ×1, 100Ω ×3, 1kΩ ×4
2. Instruments
   (1) DC power supply (Keysight E36311A)
   (2) Oscilloscope (Agilent MSOX 2014A)

III. Reading

1. Section 13-6 to 13-10 of “Microelectronics Circuits 6th edition, Sedra/Smith”.

IV. Preparation

1. Introduction
   (1) Introduction of the conversion efficiency of the power amplifier
   (2) The analysis of class-B and class-AB power amplifier

Output stage is used to provide the amplifier with a low output resistance, so that it can deliver the output signal to the load without loss of gain. Nevertheless, the linearity is also an important performance index for the signal quality. The most challenging design issue is the efficiency, it is required that the power dissipated on the transistors of the output stage must be as low as possible, and to prevent the possible damage from the over-temperature operation.

The power conversion efficiency (η) of the output stage is defined as the ratio of the load power (P_L) to the supply power(P_S) as,

$$\eta = \frac{Load\ power(P_L)}{Supply\ power\ (P_S)} \quad \text{.....(Eq. 10.1)}$$

Taking the class-A output stage as an example, the topology and the key output

waveform of the class-A output stage is shown in Fig. 10.1

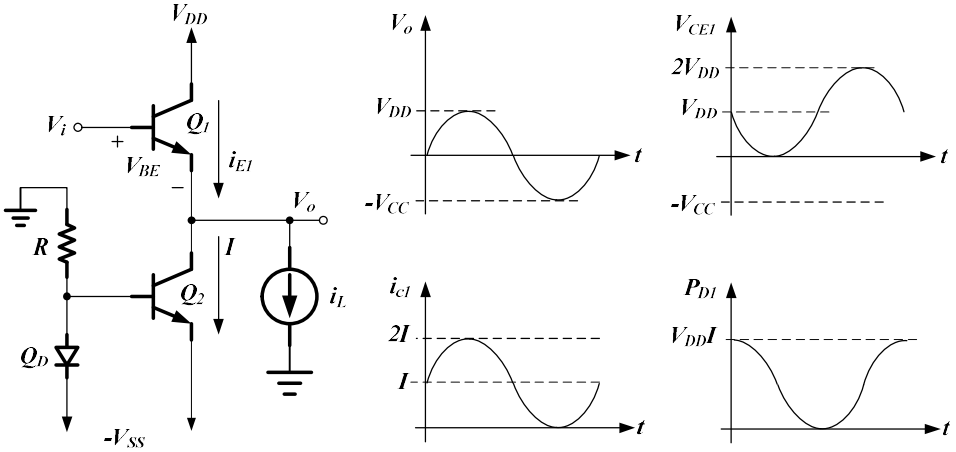

Fig. 10.1 Topology and key waveforms of the class-A output stage

The average load power of class-A can be calculated as

$$Load\ \ power(P_L) = \frac{(V_{DD}/\sqrt{2})^2}{R_L} \text{ ……..(Eq. 10.2)}$$

And the average supply power can be calculated as

$$Supply\ power(P_L) = 2V_{DD}I \text{ ……..(Eq. 10.3)}$$

And therefore the efficiency can be derived as below.

$$\eta = \frac{1}{4}\frac{V_{DD}{}^2}{V_{DD}IR_L} \text{ ……..(Eq. 10.4)}$$

Ideally, the maximum efficiency is achieved when the voltage drop on output is just right equal to the value of VDD, i.e. 25%. However, the efficiency of 25% is practically unacceptable in modern high-efficiency products, especially high-power applications, where the low efficiency may bring great heat on the devices and heat sinks may be required. In addition, the poor life time that caused by low efficiency makes the class-A output stage nearly impossible to be used on the modern products.

2. Introduction of the class-B and class-AB output stage

Class-A output stage features good linearity, but performs with poor efficiency as mentioned in the previous page. class-B output stage provides a solution for the reduction of standby power consumption, and the conversion efficiency can be improved. Topology and the transfer curve of class-B output stage is shown in Fig. 10.2.

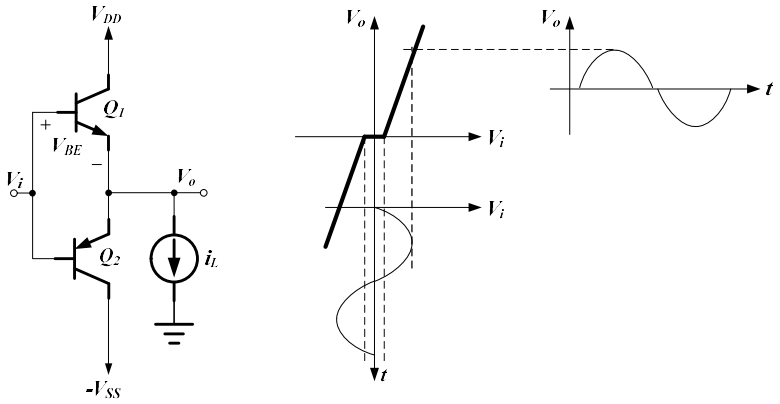

Fig. 10.2 Topology and transfer curve of the class-B output stage

When the input signal is zero, both of the transistors are off. As the input voltage crosses the threshold voltage (~0.7V), the transistor will be turned on, the current can then be flown through the transistor, and output signal will be in phase with the input signal. The load power and the supply power can be derived as below.

$$Load\ power(P_L) = \frac{(V_{DD}/\sqrt{2})^2}{R_L} \quad \text{.....(Eq. 10.5)}$$

$$Supply\ power(P_S) = \frac{2}{\pi}\frac{V_{DD}{}^2}{R_L} \quad \text{.....(Eq. 10.6)}$$

The maximum conversion efficiency can be derived then.

$$\eta_{max} = \frac{\pi}{4} \sim 78.5\% \quad \text{.....(Eq. 10.7)}$$

However, although efficiency is increased and the standby power dissipation is near zero, the existence of dead band leads crossover distortion and injects the distortion to output signal. There are some solutions for reduction of the crossover distortion, for example, amplifying the input signal through an OPAMP and feedback with the output signal. This solution corrects the output signal and reduces the crossover distortion significantly. However, finite slew rate limits the performance of class-B output stage, which inspires the idea of class-AB output stage.

In class-B output stage, having the output signal starts to change, the input signal should go up to a certain amount level, which brings crossover distortion. Class-AB output stage simply presets the input signal with an offset to eliminate the crossover distortion. The topology and the transfer curve of class-AB output stage is shown in Fig. 10.3.

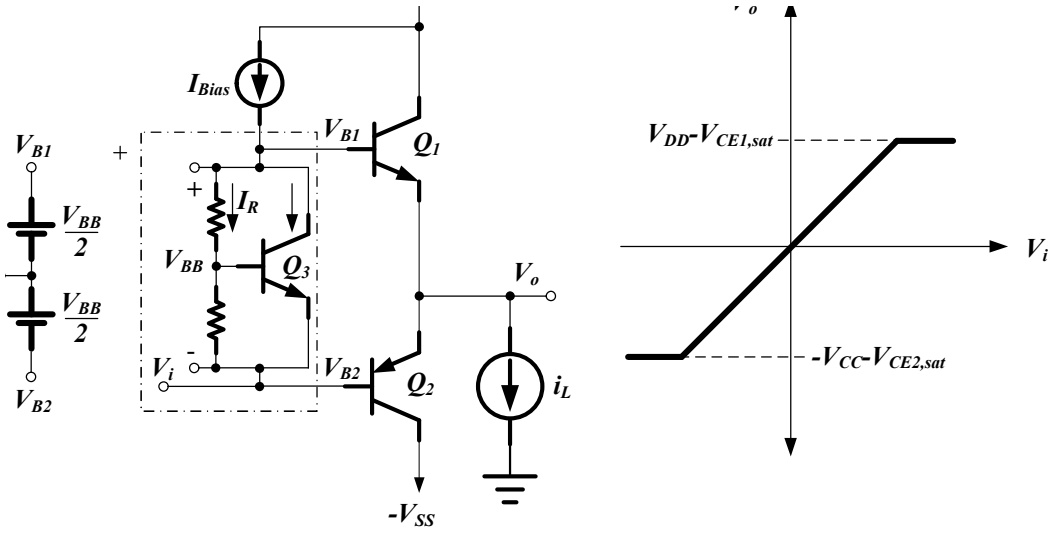

Fig. 10.3 Topology and transfer curve of the class-AB output stage

With proper design of the bias voltage on base terminal (V_{BB}), the distortion can be eliminated as shown in the transfer curve. The dash-dot line highlights a simple solution for the design of the bias circuit. The equation below shows the relationship between the ratio of the resistances and the bias voltage. According to the equation, this bias voltage can be controlled by designer.

$$I_R = \frac{V_{BE3}}{R_1} \; and \; V_{BB} = V_{BE1}\left(1 + \frac{R_2}{R_1}\right) \text{.....(Eq. 10.8)}$$

Basically, the class-AB output stage improves the crossover distortion compared with class-B, and consumes far less power losses than class-A undoubtedly. But, the conversion efficiency is inherently not good enough to be used on portable devices and high-power products. Therefore, switching power amplifiers, such as class-E, class-D power amplifier, become more and more important.

V. Exploration

1. Explore the transfer curve of class-B output stage

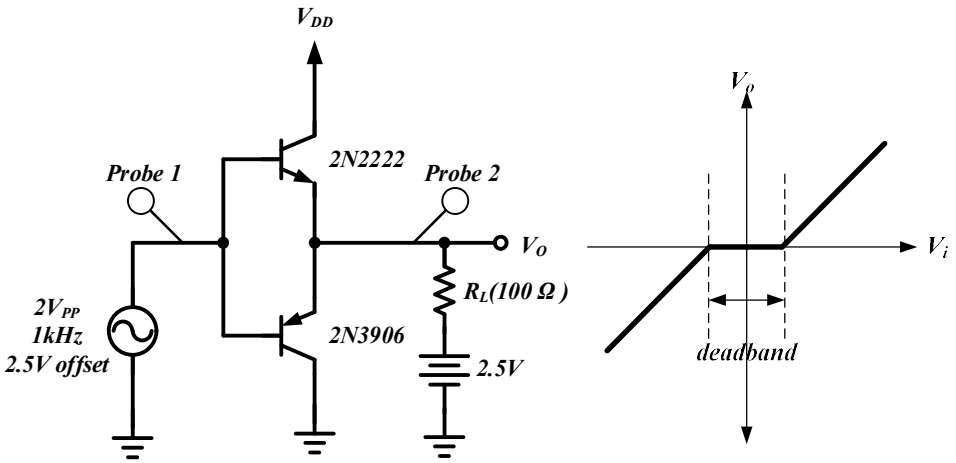

Fig. 10.4 Circuit diagram of the class-B output stage for exploration

a. Assemble the circuit of class-B topology, where we are going to measure the crossover distortion. Set VDD to be 5V, and V_{in} to be sine wave with 2Vpp, 1kHz, 2.5V offset. Please write down the value of deadband =_____V.

b. Please show the waveform of output vs. input with probes 1 & 2. Zoom in the crossover area to observe the effect of the deadband.

c. With the series connection of an 1Ω resistor between supply and the high-side transistor (2N2222). Show the current waveform on the resistor. Is this current waveform continuous? (Optional)

d. Similar to c., with the series connection of an 1Ω resistor between ground and the low-side transistor (2N3906). Show the current waveform on the resistor. Is this current waveform continuous? (Optional)

e. The peak-to-peak value output voltage is _____ V. With the load resistor to be 100Ω, the total output power is _____ mW. Record the supply current (average current) from the power supply _____, the input power is _____mW.

f. The efficiency is _____%.

2. Explore the characteristic of class-AB output stage

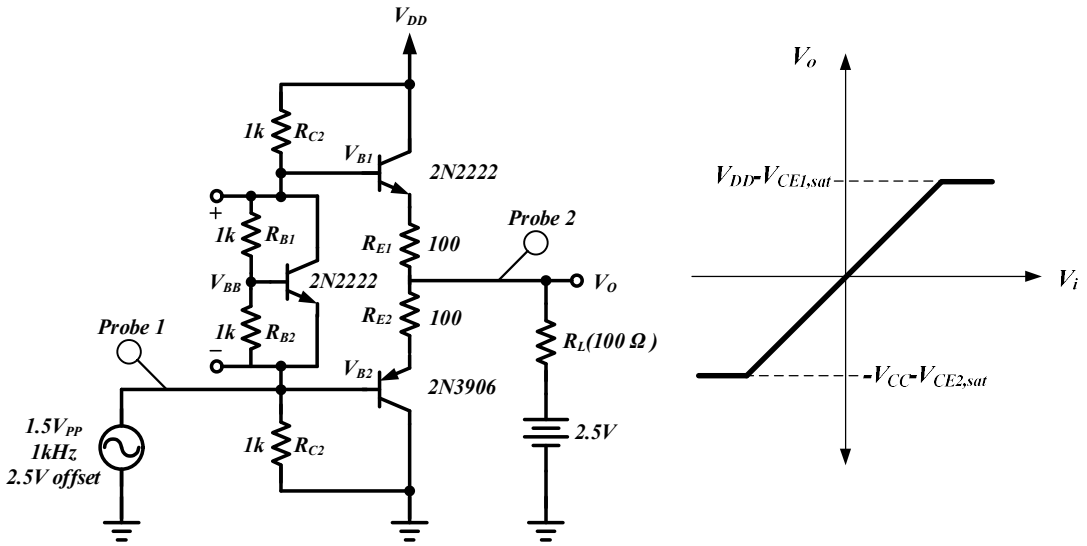

Fig. 10.5 Circuit diagram of the class-AB output stage for exploration

a. Show the waveform of output vs. input signal with probe 1 & 2.

b. Change R_{B1} into 10Ω, observe and show the output voltage waveform.

VI. Reference

1. “Microelectronic circuit”, seven edition.
2. “2N2222” datasheet.
https://www.electroschematics.com/wp-content/uploads/2009/04/2n2222-datasheet.pdf
3. “2N3906” datasheet.
https://www.onsemi.com/pub/Collateral/2N3906-D.PDF

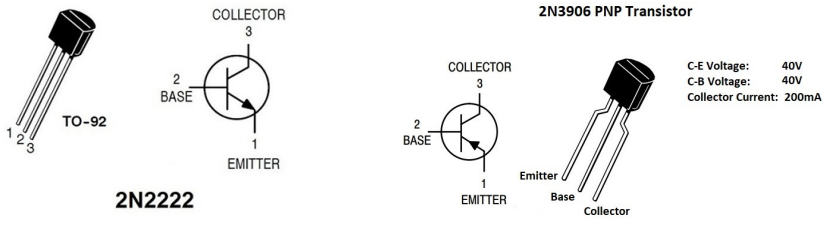

Fig. 10.6 Pin diagram of 2N2222 (NPN) and 2N3906 (PNP)

Laboratory #10 Pre-lab

Class:

Name: Student ID:

1. Explore the characteristics of class-B output stage

(1) Use PSPICE to verify the characteristics of class-B output stage as shown in Fig. 10.7, which is the same schematic as Fig. 10.4. Set VDD to be 5V, and V_{in} to be sine wave with 2Vpp, 1kHz.

Please show

(a) Current through Q1/Q2 and output current (current through R1)

(b) Output vs. input voltage waveform.

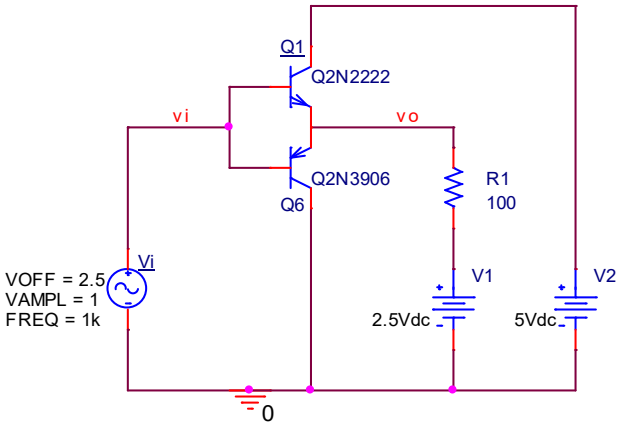

Fig. 10.7 Class-B output stage for SPICE simulation

(2) Briefly describes the characteristics of class-B output stage using these waveforms (e.g. better efficiency than class-A, and the disadvantage of crossover distortion).

2. Explore the characteristics of class-AB output stage.

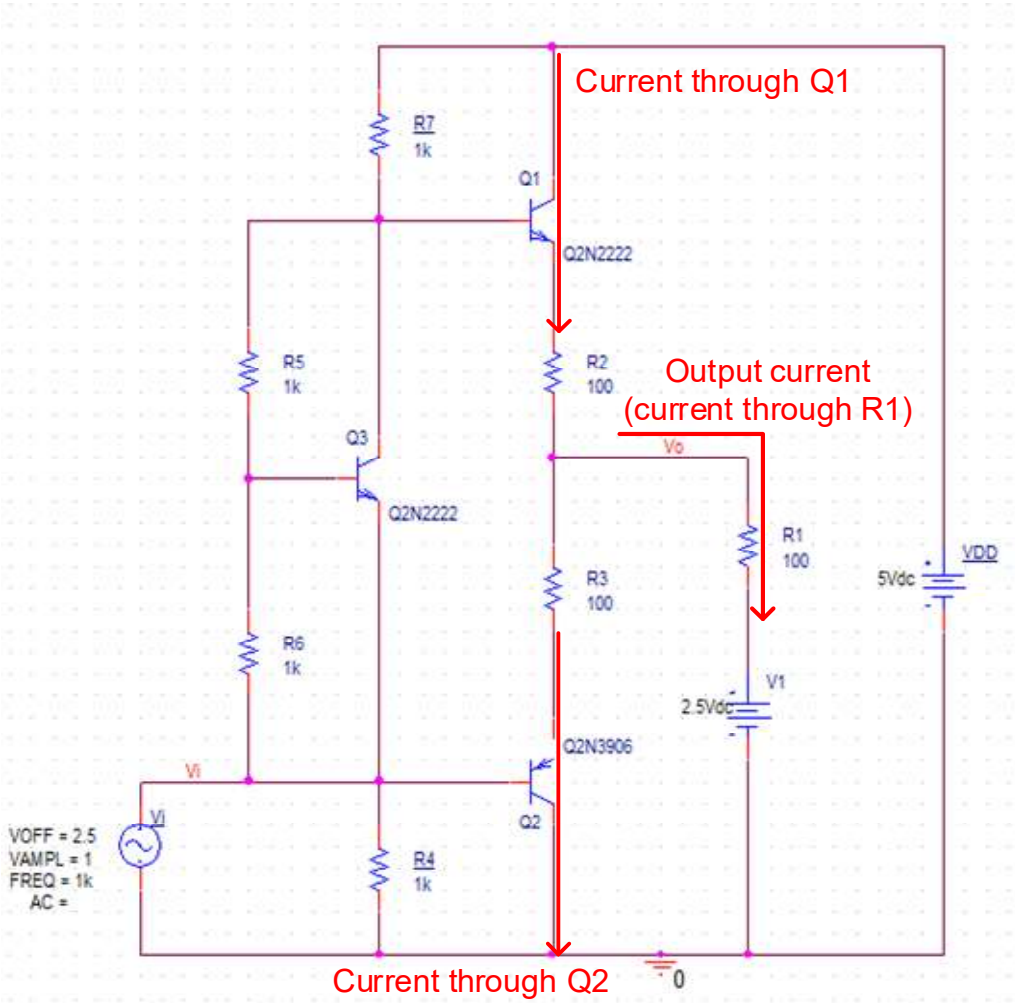

Fig. 10.8 Class-AB output stage for SPICE simulation

(1) Use PSPICE to verify the characteristics of class-AB output stage as shown in Fig. 10.8. Please show
   (a) Output vs. input voltage waveform
   (b) Current through Q1/Q2 and output current (current through R1).

(2) Briefly describes the characteristics of class-AB output stage using these waveforms (e.g. without crossover distortion).

Laboratory #10 Report

Class:
Name: Student ID:

1. Exploration 1
   (1) Deadband=_____V
   (2) Input/output voltage waveform
   (3) Calculation of the efficiency

Table 10.1

Input power	
Supply current	
Supply voltage	
Output power	
Load resistance	
(1/2)Output V_{pp}	
Efficiency	

2. Exploration 2
   (1) Output vs. input voltage waveform
   (2) Change R_{B1} into 10Ω, and shows output vs. input voltage waveform

3. Problem 1

   Briefly explain the crossover distortion occurred in class-B output stage, and why class-AB can eliminate the distortion?

4. Bonus

   In Fig. 10.5, the class-AB output stage, what is the physical meaning of R_{C1}/R_{C2}, and R_{E1}/R_{E2}?

5. Conclusion